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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/600,771	06/23/2003	Norio Ishitsuka	500.42877X00	5732

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 08/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/600,771	ISHITSUKA ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *12-44,47 and 48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,45 and 46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 6-8, 10-11 and 45-46 are rejected under 35 U.S.C. 102(b) as being anticipated by Liaw 5,972,759, newly cited.

Liaw discloses a semiconductor device, which includes :

semiconductor substrate (well) 10, figs. 1-10 and col. 3, lines 15-16, col. 6, lines 15-16, col. 4, lines 10-67,

an element isolating region 20 having a trench (STI) formed in the semiconductor substrate 1 and an embedding insulating film (an oxide) 20 which is embedded into the trench (STI) 20, fig. 1, col. 5-6,

an active region 14 formed adjacent to the element isolating region 20, in which gate insulating film (an oxide) is formed, col. 5, lines 20-33, figs. 1-2,

a gate electrode 30A, 30B is formed on the gate insulating film, col. 5, lines 20-23, col. 7, lines 15-21,

a region formed in such a manner that at least a portion of the gate electrode 30B positioned on the element isolating region 20 (figs. 1-2), and first edge surface of an upper side of embedding insulating film 20 in a first element isolating region where gate electrode 30B is positioned at a vertically higher plane than a second edge surface

20A of the embedding insulating film 20 in a second element isolating region where said gate electrode film 30B is not positioned, wherein the plane of the second edge surface of embedding insulating film 20A is positioned at a depth extended from a plane surface of said semiconductor substrate, substantially the same as or greater than that of the source and drain diffusion regions 26, figs. 2-10, col. 6, lines 10-23,

second edge surface 2A is 4000-6000 angstroms which is greater than the gate oxide of 40 angstroms, col. 6, lines 10-23,

active region 14 has impurity doped region 24/26,

an interlayer insulating film 36/40, figs. 1-10,

second edge surface 2A faces an insulating layer 50A, fig. 6,

second edge surface 2A faces a conductive plug 9A, fig. 9A.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Liaw as applied to claims 1, 3-4, 6-8, 10-11 and 45-46 above, and further in view of over Huang 6,406,987, previously cited.

Huang discloses a semiconductor device, which includes:

semiconductor substrate 1, fig. 6-7 and col. 4, lines 49+,

an element isolating region 12 having a trench (STI) formed in said semiconductor substrate 1 and an embedding insulating film 12 which is embedded into the trench (STI),

an active region formed adjacent to the element isolating region 12, in which gate insulating 14 film is formed,

a gate electrode 16 is formed on the gate insulating film 14, col. 5, lines 4+,

a region formed in such a manner that at least a portion of the gate electrode 16 positioned on the element isolating region 12 (fig. 7), and first edge surface of an upper side of embedding insulating film 12 in a first element isolating region (left hand side of fig. 7) where gate electrode is positioned at a vertically higher plane than a second edge surface of the embedding insulating film in a second element isolating region where said gate electrode film 16 (left hand side of fig. 7) is not positioned,

second edge surface is 500-1000 angstroms which is greater than the gate oxide of 40 angstroms, col. 5, lines 52+,

active region has impurity doped region 17/18,

a boundary plane (A),

an interlayer insulating film 21, fig. 8.

The difference between the references applied above and the instant claim(s) is: Liaw teaches a gate oxide and a recess region having a depth of 4000 to 6000 angstroms but does not teach the thickness of gate oxide. However, Huang teaches at col. 5, lines 1-4, the gate oxide thickness is 40 to 200 angstrom as known in the art.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to recognize that recess formed in the trench isolation region is greater than the gate oxide thickness because gate oxide thickness is known in the as a thin oxide layer to obtain a high performance transistor.

Claim 5 is rejected under 35 U.S.C 103 as being unpatentable over Liaw '759 as applied to claims 1, 3-4, 6-8, 10-11 and 45-46 above, and further in view of Liaw 5,930,633, newly cited.

The difference between the references applied above and the instant claim(s) is: Liaw '759 teaches a recess formed in the trench isolation region but does teach the recess is less than 200 nm. However, Liaw '633 teaches at col. 3, lines 66-67, the depth of recess is 1000-2000 angstroms (100-200 nm).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above Liaw '633 teachings with a recess formed in the trench isolation region having a depth of less 200 nm as taught by Liaw '633 because a shallower recess would prevent the current leakage in the contact area.

Claim 9 is rejected under 35 U.S.C 103 as being unpatentable over Liaw as applied to claims 1-8, 10-11 and 45-46 above, and further in view of Nishioka 2002/0008019, previously applied.

The difference between the references applied above and the instant claim(s) is: Liaw teaches an embedding oxide film but does not specify the oxide is a HDP oxide. However, Nishioka teaches at para. 6, an embedding oxide film is a HDP oxide. And, the selection of oxide density and coating thickness as claimed are taken to be obvious

since these are variables of art recognized importance which are subject to routine experimentation and optimization and discovery of an optimum value for a known process is obvious. In re Aller, 105 USPQ 233 (CCPA 1955). And, even if applicants' modification results in great improvement and utility over the prior art, it may still not be patentable if the modification was within the capabilities of one skilled in the art, In Re Sola 25 USPQ 433.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings with HDP oxide as taught by Nishioka because higher density of oxide increases the insulation value.

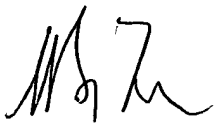
Applicant's arguments filed on July 8, 2005 have been fully considered but they are not persuasive. Because newly cited reference Liaw clearly teaches first edge surface of an upper side of embedding insulating film in a first element isolating region where gate electrode positioned is positioned at a vertically higher plane than a second edge surface of the embedding insulating film in a second element isolating region where said gate electrode film is not positioned. And, the depth of second edge surface is deeper than the source/drain regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebenttri can be reached on (571) 272-1673. The fax phone number for this Group is 571-273-8300.

hjt

8/3/2005



H. Jey Tsai
Primary Examiner
Patent Examining Group 2800